CLAIMS

1. A scan clock circuit comprising:

a clock generator for receiving a reference clock having a first frequency and providing a high frequency operating clock having a second frequency that is higher than the first frequency; and

clock control circuitry coupled to the clock generator for receiving the high frequency operating clock, the clock control circuitry comprising:

a first storage device for providing a shift/capture clock signal that is in phase with the reference clock by having first predetermined stored bits that are clocked to provide the shift/capture clock signal;

a second storage device for providing a launch clock signal for scan testing having a same frequency as the shift/capture clock frequency, the second storage device having second predetermined stored bits that provide a clock pulse so that when a period of the launch clock signal is followed by the shift/capture clock signal, a pulse-to-pulse delay between the launch clock signal and the shift/capture clock signal is equal to a nominal clock period of a predetermined clock domain to permit scan test launching and

capturing in a domain-specific at-speed period much shorter than a period of the reference clock.

2. The scan clock circuit of claim 1 wherein each of the first storage device and the second storage device each is a circular shift register.

3. The scan clock circuit of claim 1 wherein a bit length of first and second storage devices is proportional to a ratio of the second frequency divided by the first frequency.

4. The scan clock circuit of claim 1 further comprising:

multiplexing circuitry coupled to the first storage device and the second storage device, the multiplexing circuitry selectively implementing a scan test launch and capture operation by selectively providing the launch clock signal.

5. The scan clock circuit of claim 1 further comprising:

multiplexing circuitry coupled to the clock generator, the first storage device and the second storage device, the multiplexing circuitry selectively outputting either an integer divided version of the high frequency operating clock during a normal mode of operation or outputting outputs of the first storage device and the second storage device during a scan test mode of operation.

6. The scan clock circuit of claim 1 wherein bit values of the second predetermined bits are varied to vary the pulse-to-pulse delay between the launch clock signal and the shift/capture clock signal without varying the first frequency of the reference clock.

7. The scan clock circuit of claim 1 further comprising:

a third storage device for providing a second launch signal for scan testing in another predetermined clock domain, the third storage device having third predetermined stored bits that provide another clock pulse so that the pulse-to-pulse delay between the second launch signal and the shift/capture clock signal is equal to a corresponding nominal clock period of the another predetermined clock domain.

8. The scan clock circuit of claim 1 further comprising:

a first output terminal and a second output terminal for providing the high frequency operating clock in a divided form and an inverse thereof during a non-test mode, the first storage device and the second storage device being coupled to the first output terminal for providing the shift/capture clock signal and the launch clock signal at the first output terminal during a test mode; and

a third storage device for providing the shift/capture clock signal and a second launch signal for an independent clock domain during the test mode, wherein signals at the first output terminal and the second output terminal are dependent on

each other during the non-test mode and are independent of each other during the test mode.

9. The scan clock circuit of claim 1 wherein the clock generator further comprises:

feedback circuitry coupled to the first storage device for providing the shift/capture clock signal as a feedback signal to the clock generator; and

delay circuitry coupled to the reference clock and the feedback signal for ensuring that the reference clock and the feedback signal maintain a substantially same phase relationship.

10. The scan clock circuit of claim 9 wherein the feedback circuitry selectively provides the feedback signal either as an integer divided version of the high frequency operating clock during a normal mode of operation or as the output of the first storage device during a scan test mode of operation.

11. The scan clock circuit of claim 1 wherein the first predetermined stored bits comprise a plurality of bits having a first logic state and a single bit of an opposite logic state.

12. The scan clock circuit of claim 1 wherein the clock generator comprises a phase locked loop having a phase detector having a first input for receiving the reference clock and an output coupled to an input of a voltage controlled oscillator, the voltage controlled oscillator having an output coupled to the first storage device, an output of the first storage device being selectively delayed

and coupled to a second input of the phase locked loop as a feedback signal, the output of the first storage device being selectively delayed to maintain a substantially same phase between the reference clock and the feedback signal.

13. The scan clock circuit of claim 12 wherein the shift/capture clock signal and the launch clock signal of the predetermined clock domain are selectively delayed to maintain a substantially same phase with the feedback signal.

14. The scan clock circuit of claim 1 further comprising:

an input for receiving an external scan enable signal enabling either functional clocking or scan shifting in a target circuit;

a third storage device for providing a scan enable signal for scan testing, the third storage device having third predetermined stored bits correlated with the first predetermined stored bits; and

enable control circuitry coupled to the third storage device, the enable control circuitry using the third predetermined stored bits to provide an internal scan enable signal and allowing the internal scan enable signal to change state only at a predetermined phase of the reference clock signal.

15. The scan clock circuit of claim 1 further comprising:

an input for receiving a launch control signal used only in a scan test mode; and

control circuitry coupled to the first storage device for using the first predetermined stored bits to provide an internal launch

select signal and allowing the internal launch select signal to change state only at a predetermined phase of the reference clock.

16. A method of scan testing a target circuit having at least one clock domain comprising:

receiving a reference clock;

providing a shift/capture clock signal to the target circuit, the shift/capture clock signal being in phase with the reference clock; and

providing a launch clock signal for scan testing having a phase relationship relative to the shift/capture clock signal such that when a period of the launch clock signal is followed by the shift/capture clock signal, a pulse-to-pulse delay between the launch clock signal and the shift/capture clock signal is equal to a nominal clock period of the at least one clock domain to permit scan test launching and capturing in a domain-specific at-speed period much shorter than a period of the reference clock.

17. The method of claim 16 further comprising:

implementing the target circuit with a plurality of clock domains and providing a plurality of launch clock signals equal in number to the plurality of clock domains wherein the phase relationship of each launch clock signal relative to the shift capture clock signal is such that a pulse-to-pulse delay

between each of the plurality of launch clock signals and the shift/capture clock signal is equal to a nominal clock period of each of the plurality of clock domains to permit scan test launching and capturing at-speed in each of the plurality of clock domains.

18. The method of claim 16 further comprising:

generating first and second output signals at first and second output terminals wherein the first and second output signals are dependent on each other by being inverses during a non-test mode and the first and second output signals are independent of each other during a test mode.

19. A scan clock circuit comprising:

a clock generator for receiving a reference clock having a first frequency and providing a high frequency operating clock having a second frequency that is higher than the first frequency;

a global storage device coupled to the clock generator for receiving the high frequency operating clock, the global storage device storing a sequence of state values;

a first local storage device for storing a phase control signal;

clock waveform generation circuitry having a first input coupled to the global storage device for receiving the sequence of state values, a second input coupled to the first local storage device for receiving the phase control signal, a control input

for receiving a test control signal, and an output for providing a scan test clock having the first frequency, the scan test clock generating shift and capture cycles having a pulse of predetermined phase and duration when the test control signal is negated and generating a launch cycle of the scan test clock when the test control signal is asserted and having a pulse of differing phase that creates a pulse-to-pulse delay between the launch cycle and an immediately following capture cycle that is equal to a nominal clock period of a predetermined clock domain to permit scan test launching and capturing in a domain-specific at-speed period much shorter than a period of the reference clock; and

output logic circuitry coupled to the high frequency operating clock and to the clock waveform generation circuitry, the output logic circuitry providing a divided version of the high frequency clock during a normal mode of operation and providing the scan test clock during a test mode of operation.

20. The scan clock circuit of claim 19 wherein the pulse of differing phase generated by the clock waveform generation circuitry during the launch cycle of the scan test clock has a phase that is determined by both the sequence of state values and the phase control signal.

21. The scan clock circuit of claim 19 wherein the phase control signal further determines pulse duration of the scan test clock during the launch cycle.

22. The scan clock circuit of claim 19 wherein the output logic circuitry provides first and second complementary clock outputs during the normal mode of operation, and provides a first scan test signal and a second scan test signal that is independent of the first scan test signal during the test mode of operation.

23. The scan clock circuit of claim 19 wherein the global storage device is a circular shift register and the sequence of state values is a plurality of bits of a first logic value and a single bit of a second, opposite logic value, the plurality of bits being correlated to a ratio of the high frequency operating clock and the first frequency of the reference clock.

24. The scan clock circuit of claim 19 further comprising:

a second local storage device for storing a second phase control signal corresponding to an additional independent clock domain; and

second clock waveform generation circuitry having a first input coupled to the global storage device for receiving the sequence of state values, a second input coupled to the second local storage device for receiving the second phase control signal, a control input for receiving the test control signal, and an output for providing a second scan test clock having the first frequency, the second scan test clock

generating shift and capture cycles having a pulse of predetermined phase and duration when the test control signal is negated, and generating a launch cycle of the second scan test clock having a pulse of differing phase from the shift and capture cycles and from the launch cycles of the clock waveform generation circuitry that creates a pulse-to-pulse delay between the launch cycle and an immediately following capture cycle that is equal to a second nominal clock period of the additional independent clock domain.